

ABSTRACT

A graphical profile map for integrated circuits on a substrate. The graphical profile map includes a depiction of die placement boundaries and shot placement boundaries for the integrated circuits on the substrate. Also included are integrated circuit property information contours, where the contours are not limited to either of the die placement boundaries or the shot placement boundaries. In this manner, three key pieces of information for the integrated circuits are presented, including integrated circuit property information, die placement, and shot placement. Because these three pieces of information are presented in a graphical form, it is much easier to interpret the information. For example, it is much easier to determine which shot and die placements have properties that are at risk, and which shot and die placements have adequate property profiles.

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